

1/9

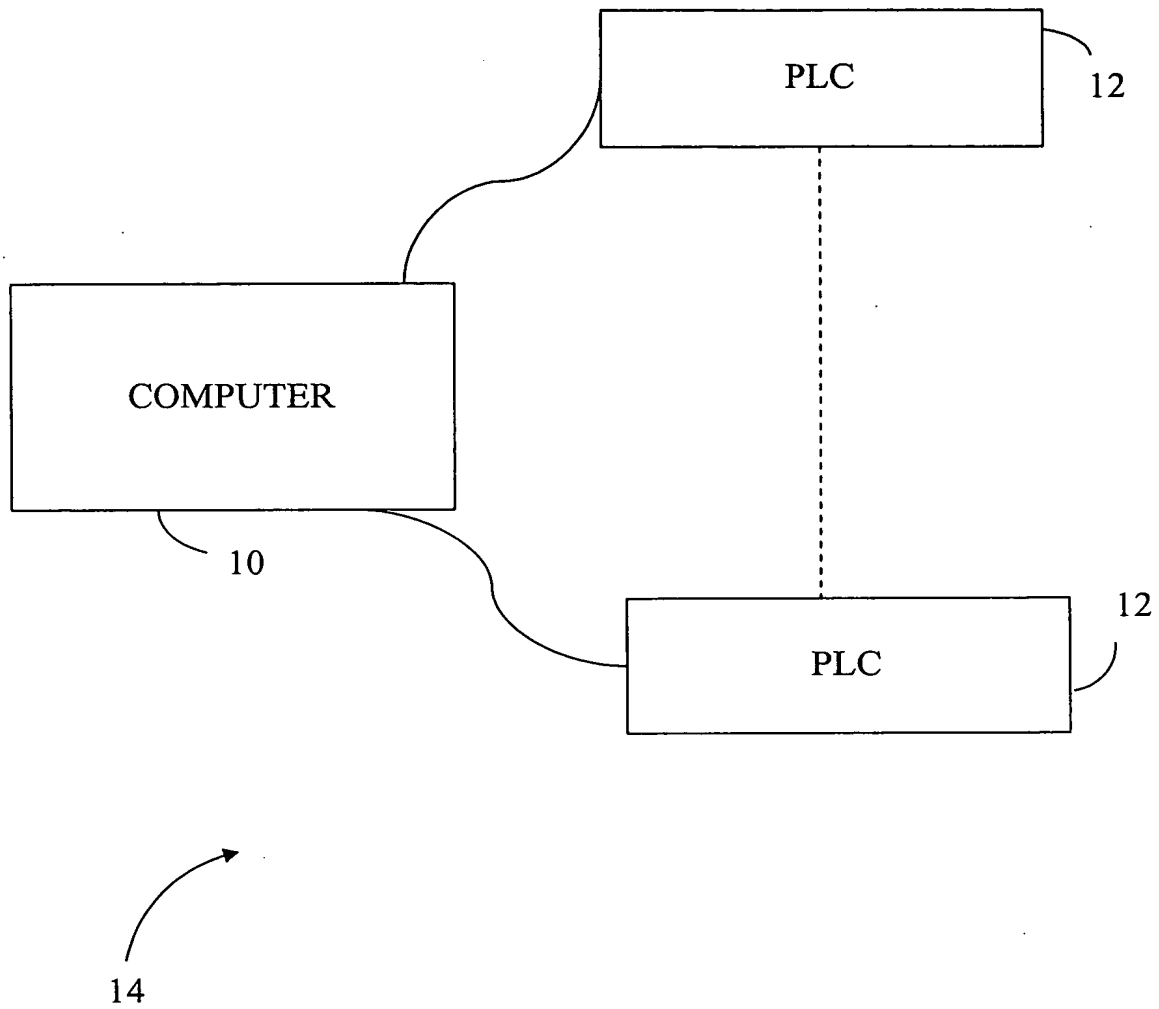


FIG. 1



# Typical Safety System Architecture

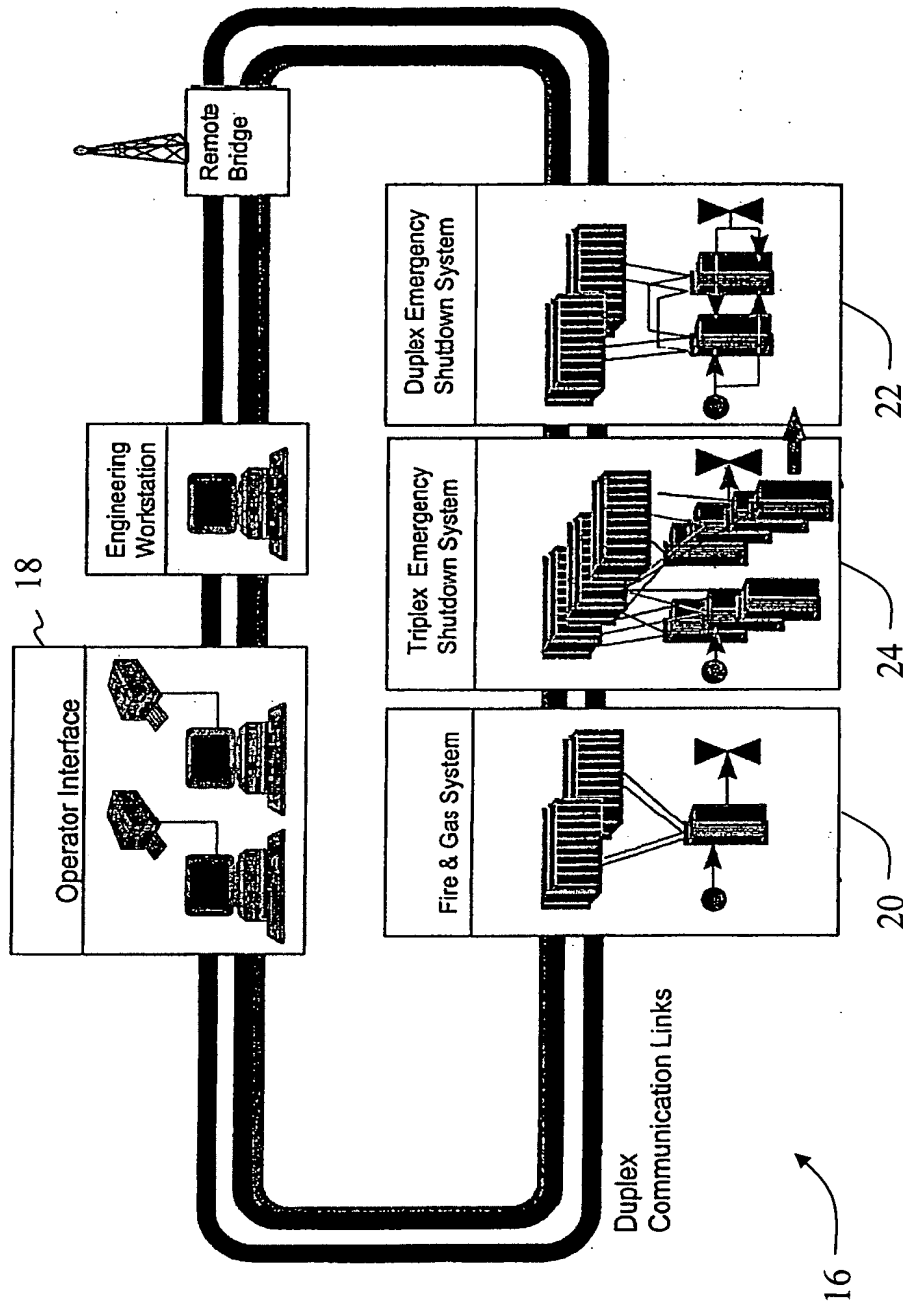


FIG. 2

3/9

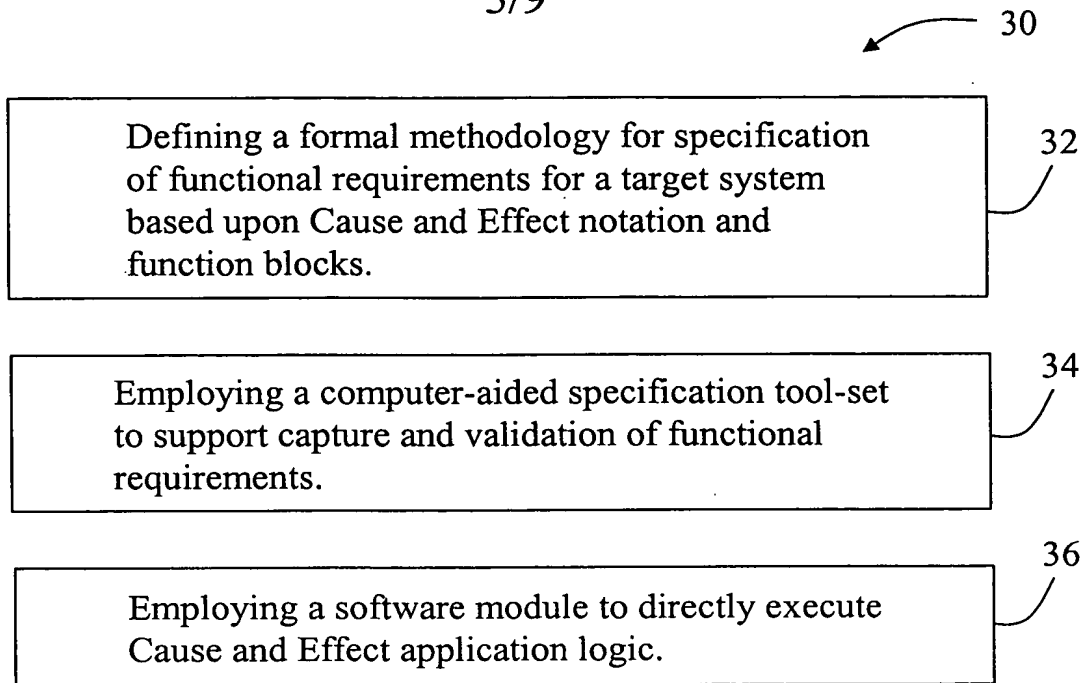


FIG. 3

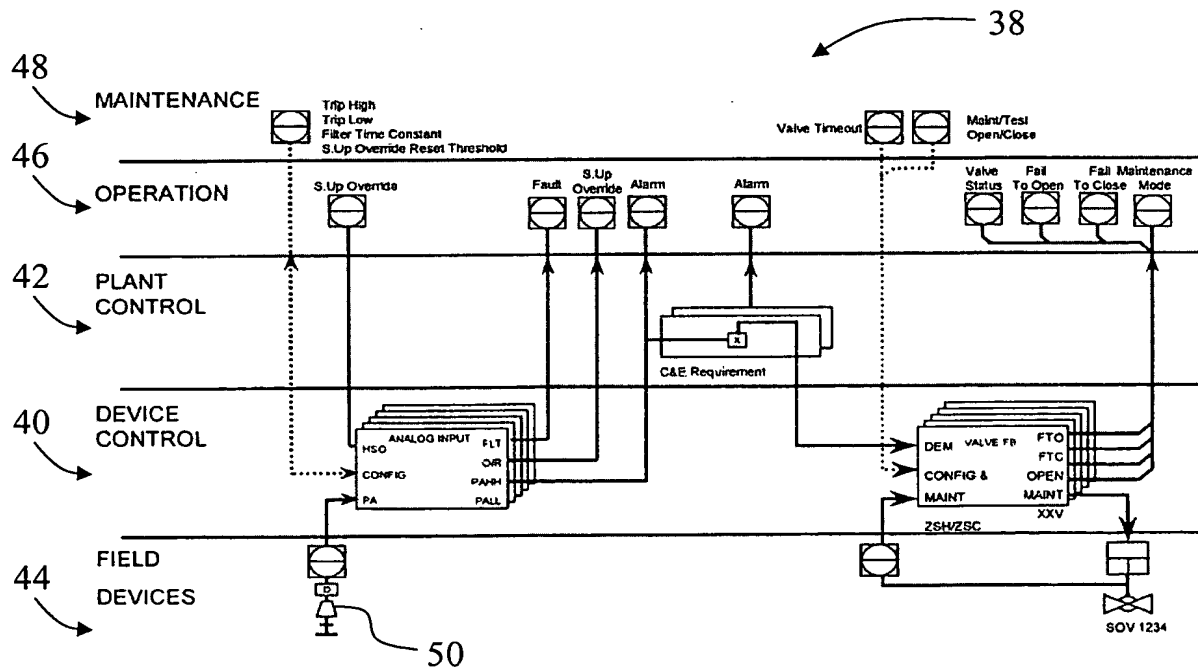


FIG. 4

4/9

54

Symbol	Name	Description
$X_n$	OR	Input term is or'ed into Gate n
$\bar{X}_n$	INV OR	Input term is inverted and or'ed into Gate N
$\&_n$	AND	Input term is and'ed into Gate n
$\bar{\&}_n$	INV AND	Input term is inverted and and'ed into Gate n
$E_n$	ENABLE	Input term is or'ed with other enables. These terms are used to enable or'ed/and'ed terms of Gate n. If no enable terms are defined then gate is enabled.
$\bar{E}_n$	INV ENABLE	Input term is inverted and or'ed with other enables. These terms are used to enable or'ed/and'ed terms of Gate n. If no enable terms are defined then gate is enabled.
$T(NN)_n$	ONTIMER	Input term is subject to on delay of NN seconds. Timer output is or'ed into group n.
$\bar{T}(NN)_n$	INV ONTIMER	Input term is inverted and subject to on delay of NN seconds. Timer output is or'ed into group n.
R	RESET	Input term resets latch. Latch set term has priority. If no reset terms are defined for a gate then gate is non-latching.
$\bar{R}$	INV RESET	Input term resets latch when false. Latch set term has priority. If no reset terms are defined for a gate then gate is non-latching.

CAUSE & EFFECT INSTRUCTION SET SUMMARY

FIG. 5

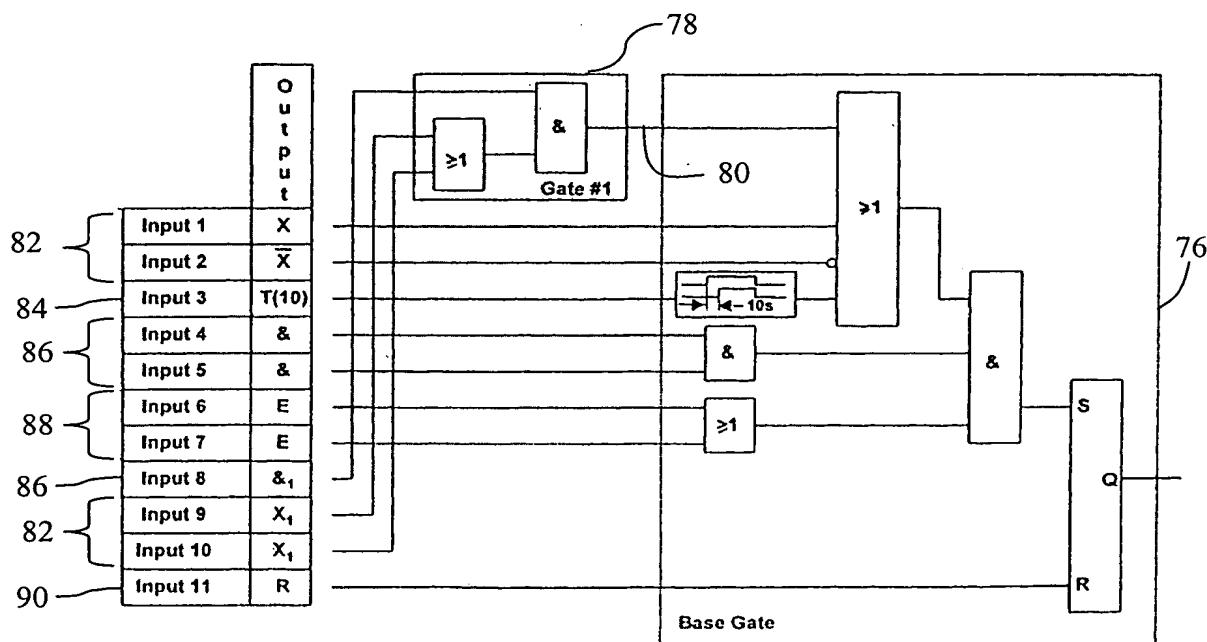


FIG. 6

5/9

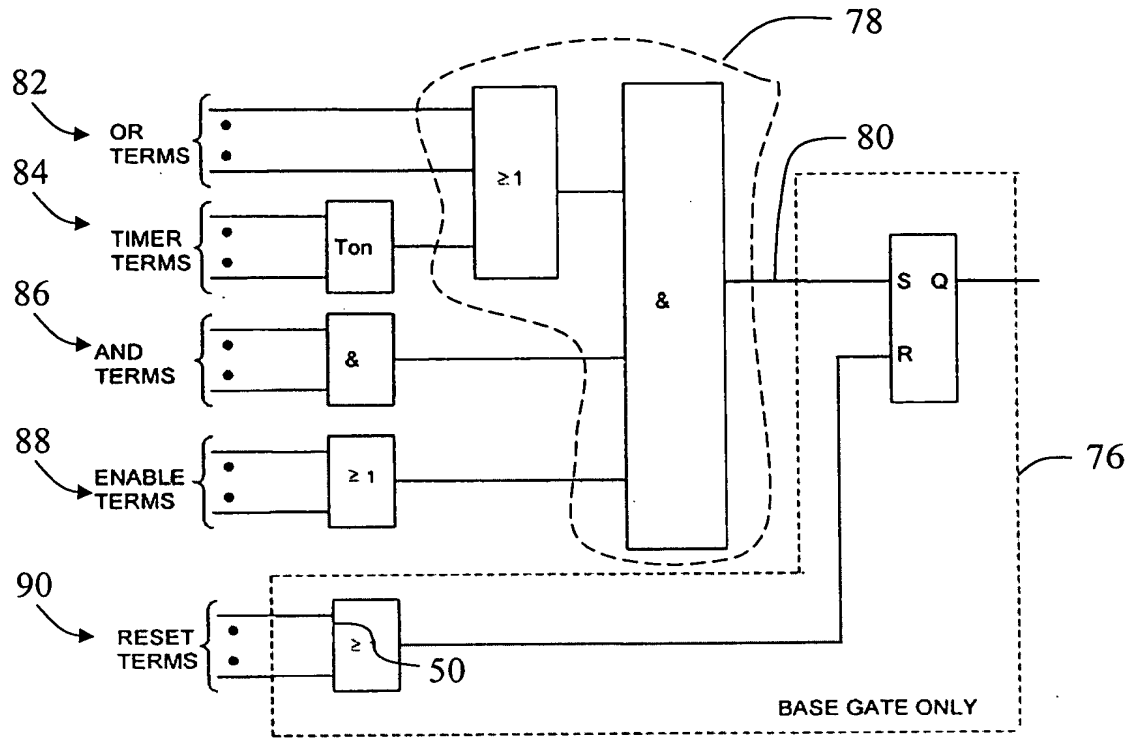


FIG. 7

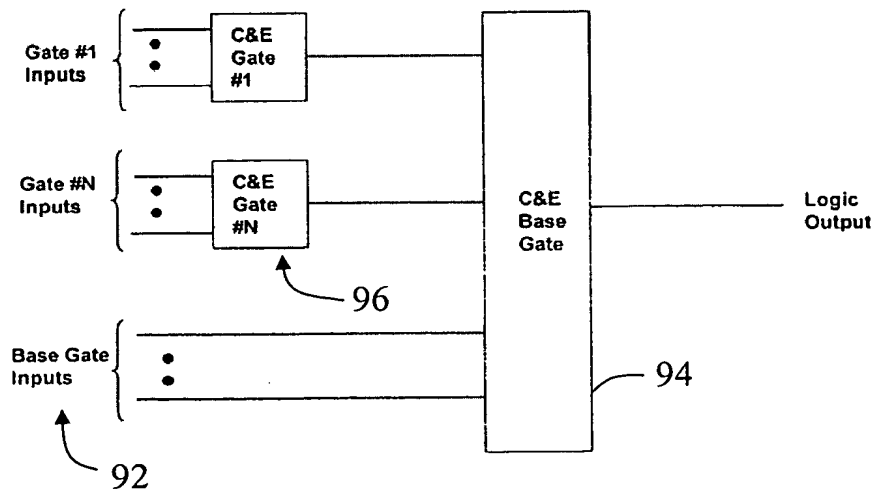


FIG. 8

6/9

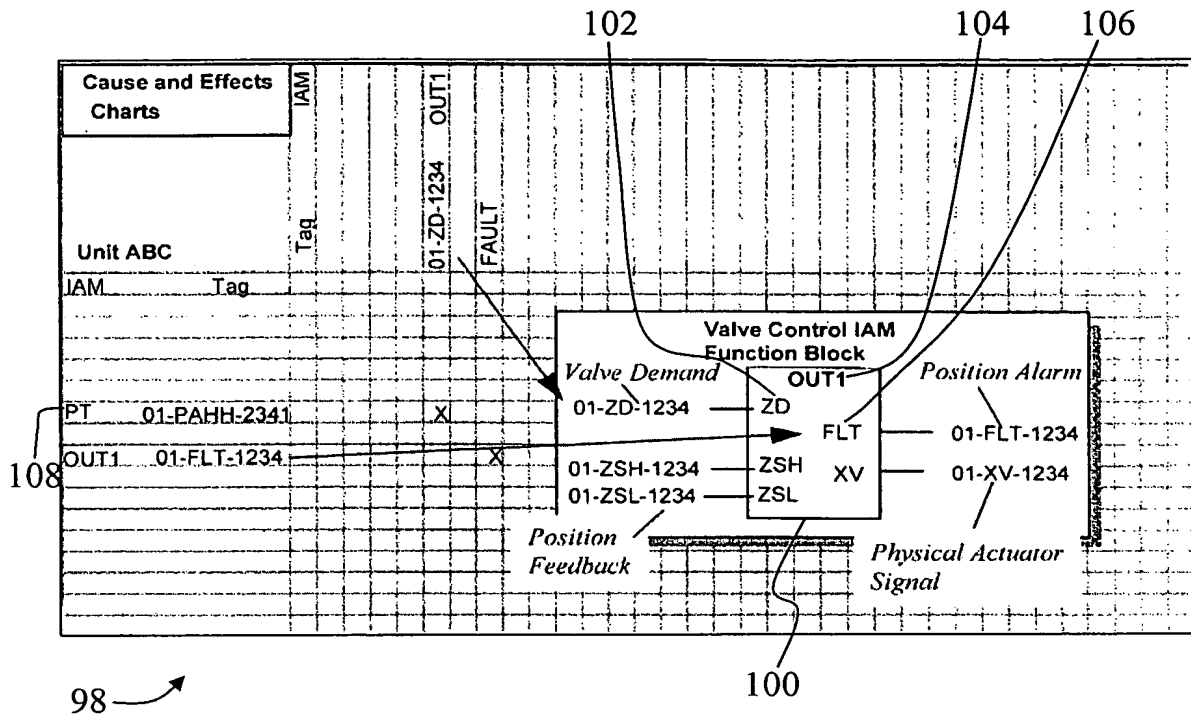


FIG. 9

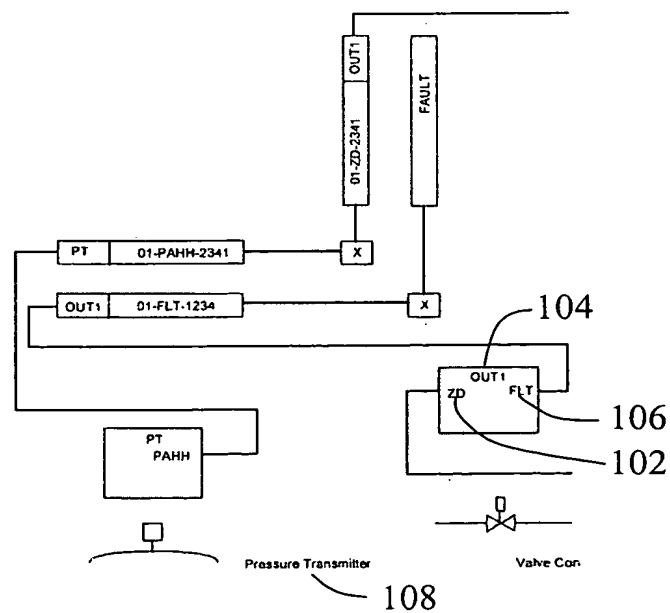


FIG. 10



8/9

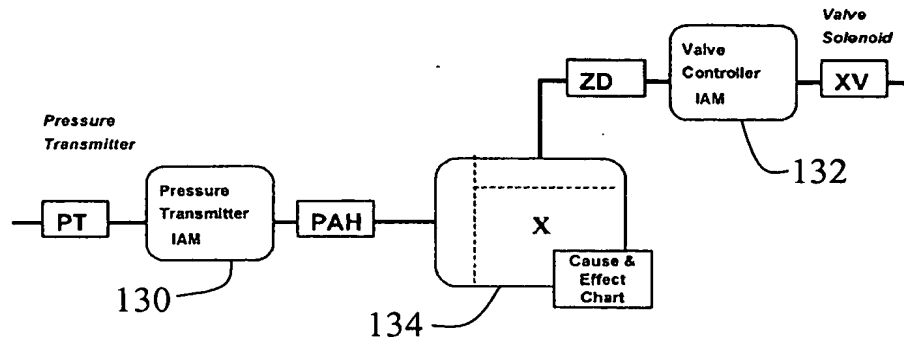


FIG. 12

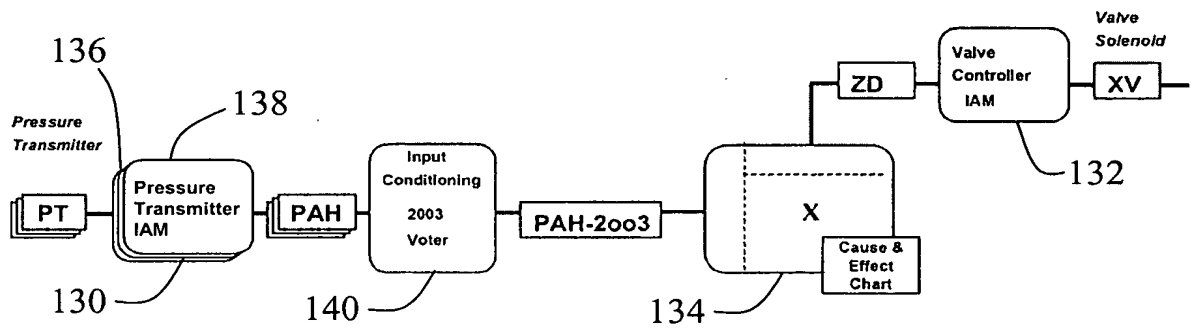
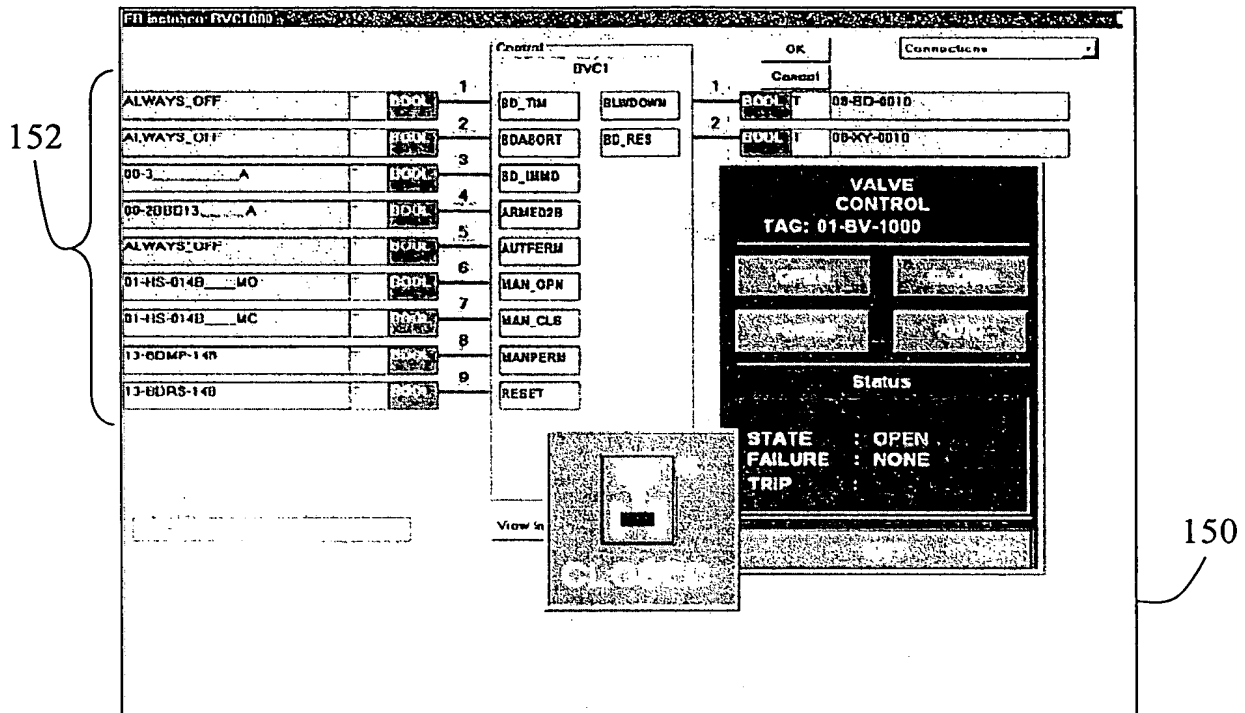


FIG. 13



9/9



FUNCTION BLOCK LOGIC TEMPLATE AND  
 ASSOCIATED HMI ELEMENTS

FIG. 14

Best Available Copy